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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/915,311	07/27/2001	Masahiro Kiyoi	NIT-285	5904
24956	7590	08/23/2004	EXAMINER	
MATTINGLY, STANGER & MALUR, P.C. 1800 DIAGONAL ROAD SUITE 370 ALEXANDRIA, VA 22314			MASKULINSKI, MICHAEL C	
			ART UNIT	PAPER NUMBER
			2113	

DATE MAILED: 08/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

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## Office Action Summary

Application No.

09/915,311

Applicant(s)

KIYOI ET AL.

Examiner

Michael C Maskulinski

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 27 July 2001.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 8 is/are allowed.
- 6) ☒ Claim(s) 1-7 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 July 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
  - 2) ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 7/27/01.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

**Non-Final Office Action**

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Nagasuka et al., U.S. Patent 6,615,364 B1.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention “by another,” or by an appropriate showing under 37 CFR 1.131.

Referring to claim 1:

a. In column 3, lines 20-25, \$ disclose that the external storage unit is used as a paging device unit. The paging device includes a primary paging device unit used as a paging device unit during a normal operation and a secondary paging device unit used as a substitution (providing said auxiliary storage with first

auxiliary storage and second auxiliary storage and operating the computer system using either of the first auxiliary storage or the second auxiliary storage)

b. In column 3, lines 4-10, \$ disclose that the control register holds various control information such as a start real address of an address translation table to be used for accessing the virtual memory (determining a location to which the address translation table is allocated when occurrence of a failure in the computer system is detected).

c. In column 4, lines 9-16, \$ disclose that areas of the virtual memory are allocated in the page unit to the main memory or primary paging device unit (determining a location in the main storage, or in the auxiliary storage, where information in the virtual-storage area is stored, which is described in the address translation table).

d. In column 4, lines 65-67 continued in column 5, lines 1-9, \$ disclose that the virtual memory information acquiring process is executed by using, as its input information, the contents of the register save area and address translation table output to the dump file by the main memory information acquiring process and the contents held in the external storage unit used as the paging device before fault occurs in the computer system (transferring the content of the virtual-storage area from the main storage to the auxiliary storage, if the content of the virtual-storage area is allocated to the main storage)

e. In column 3, lines 56-65 continued in column 4, lines 1-5, \$ disclose that the switching process is called and executed when the main memory information

acquiring process is completed. The switching process acquires the identifier of the external storage unit currently used as the paging device unit from the configuration information and changes the setting of the identifier of an external storage unit so that the secondary paging device is used as the primary paging device unit when the computer system restarts (switching the first auxiliary storage to the second auxiliary storage for use if the first auxiliary storage is used for operation, or switching the second auxiliary storage to the first auxiliary storage for use if the second auxiliary storage is used for operation).

Referring to claim 2, in column 4, lines 40-47, \$ disclose that the invalid bit indicates whether the real address is invalid or not. If the invalid bit is set to "1", it means that the real address is invalid. More specifically, the page of the virtual memory corresponding to this entry is not used or data in this page was paged out into the primary paging device unit at the page-out destination address (from among the virtual-storage pages that have been allocated to the main storage, only areas, which have been updated since the areas were allocated to the main storage, are extracted, and are then transferred from the main storage to the auxiliary storage).

Referring to claim 3, in column 5, lines 46-51, \$ disclose that the dump file holds the contents of the main memory at the time when the fault occurred, in the address sequential order (when occurrence of a failure in the computer system is detected, content of an area in the main storage, which has not been associated with the virtual storage by the address translation table, is stored in a given area in the auxiliary storage).

Referring to claims 4, 6, and 7:

- a. In column 3, lines 20-25, \$ disclose that the external storage unit is used as a paging device unit. The paging device includes a primary paging device unit used as a paging device unit during a normal operation and a secondary paging device unit used as a substitution (providing said auxiliary storage with first auxiliary storage and second auxiliary storage and operating the computer system using either of the first auxiliary storage or the second auxiliary storage)
- b. In column 3, lines 4-10, \$ disclose that the control register holds various control information such as a start real address of an address translation table to be used for accessing the virtual memory (determining a location to which the address translation table is allocated when occurrence of a failure in the computer system is detected).
- c. In column 4, lines 9-16, \$ disclose that areas of the virtual memory are allocated in the page unit to the main memory or primary paging device unit (determining a location in the main storage, or in the auxiliary storage, where information in the virtual-storage area is stored, which is described in the address translation table).
- d. In column 4, lines 65-67 continued in column 5, lines 1-9, \$ disclose that the virtual memory information acquiring process is executed by using, as its input information, the contents of the register save area and address translation table output to the dump file by the main memory information acquiring process and the contents held in the external storage unit used as the paging device

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before fault occurs in the computer system (transferring the content of the virtual-storage area from the main storage to the auxiliary storage, if the content of the virtual-storage area is allocated to the main storage). Further, in column 4, lines 40-47, \$ disclose that the invalid bit indicates whether the real address is invalid or not. If the invalid bit is set to "1", it means that the real address is invalid.

More specifically, the page of the virtual memory corresponding to this entry is not used or data in this page was paged out into the primary paging device unit at the page-out destination address (if the content of the virtual-storage area has been updated since the virtual-storage area was allocated to the main storage).

e. In column 3, lines 56-65 continued in column 4, lines 1-5, \$ disclose that the switching process is called and executed when the main memory information acquiring process is completed. The switching process acquires the identifier of the external storage unit currently used as the paging device unit from the configuration information and changes the setting of the identifier of an external storage unit so that the secondary paging device is used as the primary paging device unit when the computer system restarts (switching the first auxiliary storage to the second auxiliary storage for use if the first auxiliary storage is used for operation, or switching the second auxiliary storage to the first auxiliary storage for use if the second auxiliary storage is used for operation).

Referring to claim 5:

a. In column 3, lines 20-25, \$ disclose that the external storage unit is used as a paging device unit. The paging device includes a primary paging device unit



used as a paging device unit during a normal operation and a secondary paging device unit used as a substitution (providing said auxiliary storage with first auxiliary storage and second auxiliary storage and operating the computer system using either of the first auxiliary storage or the second auxiliary storage)

b. In column 3, lines 4-10, \$ disclose that the control register holds various control information such as a start real address of an address translation table to be used for accessing the virtual memory (determining a location to which the address translation table is allocated when occurrence of a failure in the computer system is detected).

c. In column 4, lines 9-16, \$ disclose that areas of the virtual memory are allocated in the page unit to the main memory or primary paging device unit (determining a location in the main storage, or in the auxiliary storage, where information in the virtual-storage area is stored, which is described in the address translation table).

d. In column 4, lines 65-67 continued in column 5, lines 1-9, \$ disclose that the virtual memory information acquiring process is executed by using, as its input information, the contents of the register save area and address translation table output to the dump file by the main memory information acquiring process and the contents held in the external storage unit used as the paging device before fault occurs in the computer system (transferring the content of the virtual-storage area from the main storage to the auxiliary storage, if the content of the virtual-storage area is allocated to the main storage). Further, in column 4, lines

40-47, \$ disclose that the invalid bit indicates whether the real address is invalid or not. If the invalid bit is set to "1", it means that the real address is invalid.

More specifically, the page of the virtual memory corresponding to this entry is not used or data in this page was paged out into the primary paging device unit at the page-out destination address (if the content of the virtual-storage area is allocated to the main storage, and if the content of the virtual-storage area has been updated since the virtual-storage area was allocated to the main storage).

e. In column 3, lines 56-65 continued in column 4, lines 1-5, \$ disclose that the switching process is called and executed when the main memory information acquiring process is completed. The switching process acquires the identifier of the external storage unit currently used as the paging device unit from the configuration information and changes the setting of the identifier of an external storage unit so that the secondary paging device is used as the primary paging device unit when the computer system restarts (switching the first auxiliary storage to the second auxiliary storage for use if the first auxiliary storage is used for operation, or switching the second auxiliary storage to the first auxiliary storage for use if the second auxiliary storage is used for operation).

***Allowable Subject Matter***

3. Claim 8 is allowed.
4. The following is a statement of reasons for the indication of allowable subject matter: the prior art does not teach or reasonably suggest restoring the address

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translation table, which has been saved in the first auxiliary storage, in the main storage before switching the first auxiliary storage, which is working, to second auxiliary storage.

### ***Conclusion***

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent 5,043,871                      Nishigaki et al.

JP 406348528 A                              Kobayashi et al.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C Maskulinski whose telephone number is (703) 308-6674. The examiner can normally be reached on Monday-Friday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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MM

  
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